PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Hiroji AGA et al. Group Art Unit: 2813

Application No.: 10/507,175 Examiner: C. RODGERS

Filed: September 10, 2004 Docket No.: 121026

For: METHOD OF PRODUCING SOI WAFER AND SOI WAFER

DECLARATION UNDER 37 C.F.R. §1.132

I, Hiroji AGA, a citizen of Japan, hereby declare and state:

1. I have a degree in material science which was conferred upon me by Hiroshima University in Japan in 1994.

2. I have been employed by Shin-Etsu Handotai Co. since 1994 and I have had a total of 13 years of work and research experience in research and development of SOI wafers.

3. I am a named inventor in the above-captioned patent application. I am familiar with the patent application.

4. I have a professional relationship with the Assignee, Shin-Etsu Handotai Co., Ltd., of the above-identified patent application. In the course of that professional relationship, I received compensation directly from Shin-Etsu Handotai Co., Ltd. for my work relating to research and development of SOI wafers. I am being compensated for my work relating to research and development of SOI wafers.

5. I and/or those under my direct supervision and control have conducted the following experiments.

The experimental results demonstrate that SOI wafers produced by the recited method of the present claims (in which an oxide film is formed with a thickness of 100 nm or more

and then the buried oxide film thickness is reduced to less than 100 nm by heat treatment) achieve unexpected results in avoiding voids and blisters when compared to SOI wafers produced by a method like that of U.S. Patent No. 6,372,609 in which an oxide film is formed with a thickness of less than 100 nm.

Examples 1 and 2 are the same SOI wafers as Examples 1 and 2 in the present application. The amount of generation of voids and blisters before heat treatment was evaluated and is set forth in Table 1 below. Voids and blisters are illustrated in Fig. 3 of the present application, and the amount of such voids and blisters was determined by visual inspection of the wafer. In the process, the wafers were subjected to heat treatment at 1200°C for 4 hours (Example 1) and 14 hours (Example 2), and the amount of generation of voids and blisters was again evaluated as shown in Table 1.

First Comparative SOI wafers (Comparative Examples 1' and 2') were produced under the same conditions as Comparative Examples 1 and 2 in the present application. The wafers of Comparative Examples 1' and 2' were subjected to heat treatment at 1200°C for 4 hours, and the amount of voids and blisters in the wafers was evaluated before and after the heat treatment. The results for Comparative Examples 1' and 2' are also shown in Table 1.

Second Comparative SOI wafers (Comparative Examples 1" and 2") were also produced under the same conditions as Comparative Examples 1 and 2 of the present application. Comparative Examples 1" and 2" were subjected to heat treatment at 1200°C for 14 hours, and the amount of voids and blisters in the wafers was evaluated before and after the heat treatment. The results for Comparative Examples 1" and 2" are shown in Table 1.

Table 1

	Example 1	Example 2	Comparative Example 1'	Comparative Example 2'	Comparative Example 1"	Comparative Example 2"
Thickness of formed oxide film in total	100 nm	100 nm	80 nm	30 nm	80 nm	30 nm
Implantation energy	53 keV	50 keV	50 keV	44 keV	50 keV	44 keV
Implantation dose ($/cm^2$)	$5.5x10^{16}$	$5.5x10^{16}$	$5.5x10^{16}$	$5.5x10^{16}$	$5.5x10^{16}$	$5.5x10^{16}$
Stock removal of touch polishing	60 nm	60 nm	60 nm	60 nm	60 nm	60 nm
Thickness of SOI layer	320 nm	320 nm	320 nm	320 nm	320 nm	320 nm
Heat treatment conditions to reduce thickness of oxide film (in Ar gas atmosphere)	1200 °C 4 hours	1200 °C 14 hours	1200 °C 4 hours	1200 °C 4 hours	1200 °C 14 hours	1200 °C 14 hours
Thickness of buried oxide film after heat treatment	80 nm	30 nm	60 nm	10 nm	10 nm	0 nm
Amount of generation of voids and blisters (before heat treatment)	0	2	19	26	21	29
Amount of generation of voids and blisters (after heat treatment)	0	2	19	26	21	29

The results for Examples 1 and 2, Comparative Examples 1' and 2' and Comparative Examples 1" and 2" as shown in Table 1 indicate that the amounts of generation of voids and blisters in the SOI wafers remain unchanged from before to after the heat treatment. Thus, the results demonstrate that once voids and blisters are generated, they cannot be eliminated by heat treatment, even a longer high temperature heat treatment such as used to reduce the buried oxide layer thickness.

Additionally, the results in Table 1 demostrate that SOI wafers formed in a process using oxide films having a thickness of 100 nm or more that is reduced to 100 nm or less by heat treatment achieve unexpectedly reduced occurrences of voids and blisters compared to wafers derived from processes in which the oxide film has a thickness of less than 100 nm upon formation.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and/or imprisonment under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date: July 4th, 2007

Hiroji Aga

Hiroji AGA